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VERY LARGE SCALE INTEGRATION(VLSI) AGENDA

01	Introduction: VLSI technology trends & Performance measures and Moore's law	Class 1 - 1 hour
02	MOS devices and Circuits: MOS capacitor and MOS transistors MOS transistors: Study of depletion mode operation	Class 2 – 1 hour
03	MOS transistors: Drain current analysis, and numericals based on it Threshold voltage and numericals based on it	Class 3 – 1 hour
04	Second order effects in MOSFETs(Numericals involving Channel Length Modulation)	Class 4 – 1hour
05	Analysis of NMOS inverter circuit Analysis of CMOS inverter circuit	Class 5 – 1 hour
06	Fabrication of ICs: Lithographic fundamentals Fabrication of ICs: Fabrication of process of NMOS and PMOS transistor	Class 6 – 1 hour

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07	CMOS fabrication: N-well and P-well Twin tub processes	Class 7 - 1 hour
08	Latch up in CMOS and its prevention SOI process MOS Circuit Design & Layouts: Pass transistors and transmission gates.	Class 8 – 1 hour
09	Implementation of Boolean functions and combinational circuits using switch logic	Class 9 – 1 hour
10	BiCMOS inverters and Logic circuits Pseudo NMOS inverter with derivation of Zpu/Zpd ratio	Class 10 – 1hour
11	Dynamic and clocked CMOS inverters, clocking strategies Stick diagrams, design rules and layouts, Flip flops and sequential circuits	Class 11 – 1 hour
12	Sheet resistance, standard unit of capacitance, estimation of delay in NMOS and CMOS inverters	Class 12 – 1 hour

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13	Driving of large capacitive loads Euler network, and Scaling of MOS circuits	Class 13 - 1 hour
14	Static and dynamic memory cells: RAM,ROM like NOR and NAND ROM Static and dynamic memory cells: EPROM, EEPROM and flash memory	Class 14 – 1 hour
15	Super buffers, power dissipation in CMOS Design strategies, design issues and structured approach, Structured approach: design examples	Class 15 – 1 hour
16	Structured approach: Bus arbitration logic, Shifter as design example Structured approach: ALU as design example, Parity generator	Class 16 – 1hour
17	Design of logic circuits using PLA : combinational and sequential logic FinFET-Fabrication and operation	Class 17 – 1 hour
18	Compound Semiconductor - Fabrication and operation Tunnel FET, spintronic device	Class 18 – 1 hour